Fermi National Accelerator Laboratory

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AN MC68000 MULTIBUS-COMPATIBLE COMPUTER BOARD

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1.0 Introduction

A Motorola MC68000-based single board computer has been developed for use in Fermilab accelerator control applications. Because it is compatible with the Multibus* specification this computer will operate in conjunction with other commercially available Multibus memory, I/O,peripheral, and processor boards. The Multibus specification is being considered for adoption by the IEEE as standard number IEEE-796. The board was developed because no 68000-Multibus CPU board is commercially available. The purpose of this note is to document the features and options of this board. A photograph of the board, a block diagram, and the circuit diagram are given in Figures 1.1, 1.2, and 1.3, respectively.

2.0 Overview of the Computer Board

2.1 Summary of Features

The 68000 computer board provides the following features:

a. Multibus compatible
b. On-board RAM
c. On-board ROM
d. Two asynchronous serial ports
e. Four programmable parallel I/O ports
f. Three 16-bit programmable timers
g. One megabyte (20-bit) off-board memory addressing.
h. Programmable memory mapping.
i. Multi-Master bus arbitration.

2.2 Power Requirements

The computer receives its power from the Multibus. The entire board operates on +5 volts with the exception of the RS232 interface that uses $\pm$ 12 volts. Power requirements are:

+5 V - 2.5 A
+12V - 50 mA
-12V - 25 mA

2.3 General Description

The 68000 board is designed to be both simple and flexible. Only general purpose memory and I/O are included on the board. Special purpose facilities such as disk controllers can be added as additional Multibus boards.

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*Multibus is a trademark of the Intel Corporation.

2.3.1 Serial Interface

Two asynchronous serial ports are included. The baud rates are individually switch selectable for standard frequencies between 50 and 19,200 baud. Both ports are initially configured to transmit and receive without handshake lines although jumper options are provided for the normal CTS, RTS and DCD interface signals. All signals are received and transmitted through RS232 compatible buffers.

2.3.2 Timer

A three channel 16-bit timer (MC6840) is available on the board. This timer is intended primarily for processor housekeeping. No connector is provided to input or output signals to or from the timer - the clock, gate and output pins for each timer are terminated on wire wrap posts near the chip. For normal applications the timer counts the processor "E" clock, a 800 kHz square wave generated by the 68000.

2.3.3 Parallel Interface

Two 6821 Peripheral Interface Adapters (PIA) are provided. All the interface lines are brought out to individual 26 position card edge connectors. Five volt power is also brought to each of these two connectors. The two 8-bit PIA's are configured to straddle the 16-bit data bus so that 16-bit data may be transferred using the A ports or B ports of both PIA's.

2.3.4 Bus Arbitration

The bus arbitration circuit allows this computer to share the Multibus with other processors or master controllers. Memory that resides on this board is not available to other masters on the Multibus. With this design processors with the same memory map can share the Multibus without interference.

2.3.5 On Board Memory

The sixteen memory sockets contained on the board are organized as eight pairs of byte-wide memories. Jumpers are provided to accommodate either RAM or ROM memories. Compatible memories are Mostek 4118 (1K byte) and 4802 (2K byte) RAM chips or 2716, 2532 and 68764 PROM's containing 2K, 4K, and 8K bytes respectively. Each socket pair is separately selected with its own base address and range. This design allows any mix of RAM or ROM to be chosen to fit a particular application.

2.3.6 Address Decoding and Memory Mapping

The memory allocation is completely determined by programmable decoders using Programmable Array Logic (PAL) devices. The first level decoder has the upper address lines A19 through A12 as input. It determines if the address corresponds to on-board memory or I/O, or

off-board memory or I/O. If an on-board memory access is detected the on-board memory select PAL is enabled. This PAL has address lines A17 through A10 as input and has eight select lines as output. The bases and ranges of the on-board memory blocks are determined by the first PAL; the base and range of addresses of individual socket pairs are determined by the second PAL.

Similarly, if the present address is determined to be an on-board I/O address, the I/O select decoder is enabled. This decoder is a 256 by four-bit PROM that selects the on-board peripheral chips - the PIA's, ACIA's, and the timer.

Any address determined to be an off-board memory or I/O access, will begin a bus arbitration cycle. Once access is achieved the appropriate Multibus memory or I/O, read or write command will be asserted according to the Multibus data transfer specification.

2.3.7 Transfer Acknowledge and Bus Errors

The 68000's data transfers are asynchronous - a Data Transfer Acknowledge (DTACK) signal is required to complete an access. For Multibus cycles this signal is provided naturally by the Multibus Transfer Acknowledge (XACK). For on-board memory cycles a DTACK generator is provided to terminate the cycle a fixed time after an on-board memory access is started. The delay time is selectable to match the access time of the on-board memory chips. All on-board DTACK delays are the same whether RAM or ROM is selected. The timing for the XACK signal for Multibus transfers is controlled by the individual Multibus card that is being accessed.

In the event that unassigned memory is accessed, no DTACK will be generated. An on-board "watchdog" timer is included to detect a lack of response, and a pulse is generated that may be jumpered to the 68000 Bus Error input pin. A signal asserted on this pin will initiate Bus Error Exception processing and a user-supplied routine is executed to allow the system to analyze and report or recover from this condition. Notice that the 68000 itself will patiently wait forever, if desired, for a DTACK response to come. No restriction is placed on the speed of response of the addressed memory or device. The watchdog timer delay is user-determined and its implementation is optional. It is included to keep the system from hanging up if no response is received.

Conditions that will cause a bus error are:

a) Memory addresses that are not assigned in the address decoder PAL.
b) Access to off-board addresses that have no responding memory or device (not plugged in, or not working).

An access to an on-board memory address will not cause a bus error even if a memory chip is not installed. On-board I/O uses the 68000 synchronous transfer capability and no DTACK is required.

2.3.8 Function Codes

The 68000 processor outputs three function code bits, FC0,FC1,FC2, to allow external circuitry to know the internal operating mode of the processor. The state of these outputs indicates whether the processor is in the supervisor or user state, whether the present access is a program or data reference, and if the processor is responding to an interrupt. These function codes bits are used as inputs to the Address Decode PAL so it is possible to separate the various memory spaces as desired. For example, a block of Supervisory RAM may be assigned that disallows access by user programs. The function code information is used after reset to retrieve the starting values for the supervisor stack pointer and the program counter. Because these values are accessed starting at location zero in supervisory program space, they may be read from a different memory socket from the rest of the vectors that also reside in the first 256 bytes of memory, but in supervisory data space. This feature allows the exception and interrupt vectors to be in RAM while the initial values for the stack pointer and program counter are in PROM.

2.3.9 Clock

Four clocks are generated on-board.

2.3.9.1 Processor Clock

A Motorola LOCO II 16 MHz oscillator provides the processor clock. The 16 MHz is divided by two to generate the 8 MHz for the 68000 Clock input pin. The 16 MHz clock is used directly for the DTACK generator.

2.3.9.2 Baud Rate Clock

Two options exist for the baud rate clock. A 5.0688 MHz crystal (XTAL 2) and a COM 5016 baud rate generator or a pin -compatible Motorola K1135A baud rate generator. The Motorola part includes a crystal so XTAL 2 is not needed. The baud rate selection for the host and the terminal ACIA's is made by the dual four-bit piano-dip switch SW2.

2.3.9.3 Bus Clock and Constant Clock

A 10 MHz oscillator, consisting of XTAL1 and a 74S124, generates a clock to be used as the Multibus BCLK and CCLK. Because only one card can assert these signals, jumpers are provided to connect these clocks to the bus. With the jumpers removed, the card uses the BCLK and CCLK generated by another master in the Multibus bin.

2.3.9.4 The E Clock

The 68000 outputs an E clock that is one-tenth the input clock frequency. Synchronous transfers to the on-board Motorola peripherals are made using this clock. Accordingly, it is connected to the enable input of the PIA, ACIA and timer chips. This frequency is used by the timer chips when it is configured to count the E clock.

2.3.10 Interrupts

The 68000 provides for seven levels of prioritized auto-vectored interrupts. A 74148 priority encoder is included for inputting low active interrupts. The output of the 74148 directly connects to the IPL0, IPL1, IPL2 inputs of the processor. Interrupt outputs from the on-board peripherals and the Multibus interrupt lines must be connected to the priority encoder by the user. Wire wrap pins are provided for each interrupt source.

The 68000 feature of reading an interrupt vector number from the interrupting device has not been implemented on this board.

2.3.11 Status Indicators

Two LED indicator lights are included to show when the processor is in the supervisor mode and when the processor is halted.

3.0 User Definable Options

This section describes the jumpers and options included on the board.

3.1 Serial I/O Options

3.1.1 Handshake Signal Jumpers

The serial I/O is implemented using 2 Motorola 6850 ACIA chips. When these are connected using ribbon cable and compatible 26 pin card edge/25 pin "D" connectors, the pinout of the "D" connector is the same as an RS232 modem. That is, they directly drive an RS232 terminal. The pinout of the connector is shown in Section 4. Both serial ports connected the same and both are configured by traces on the board to operate without handshake. TX and RX clocks are connected together. To enable CTS, DCD, and RTS, the required cut-traces and installed jumpers are given below:

Control Line	Terminal	Host
CTS	Cut trace at J9 Add jumpers P2-J9 P1-P5	Cut trace at J5 Install jumper at J5
DCD	Cut trace at J10 Add Jumpers P4-J10 P3-P6	Cut trace at J6 Install jumper at J6
RTS	Cut trace at J7 Install jumper at J7	Cut trace at J8 Install jumper at J8

3.1.2 Baud Rate Selection

A dual 4-bit baud rate select piano-dip switch is located in the upper left corner of the board. On this switch a "1" is up (open); a "0" is down (close). The switch setting and the associated baud rates are given below. The "DCBA" label matches the silk screen lettering on the board. These switch definitions assume that the ACIA is programmed for the divide by sixteen mode so that the actual clock frequency applied to the chip is 16 times the baud rate.

Switch Setting "DCBA"	Baud Rate
0000	50
0001	75
0010	110
0011	134.5
0100	150
0101	300
0110	600
0111	1200
1000	1800
1001	2400
1011	3600
1100	4800
1101	7200
1110	9600
1111	19200

3.2 Bus Error Jumpers

Jumper J12 connects the output of the watchdog timer to an encoder that operates the BERR and HALT lines of the 68000. If J12 is not installed no bus error is received and the processor continues to execute WAIT states indefinitely. In this case the address and data lines are static and can be examined at leisure. This is a useful mode for debugging.

J12 can be installed in two ways as shown in Figure 3.1. When J12 is configured as in 3.1A a bus error will occur causing bus error exception processing to be executed.

For J12 installed as in 3.1B the HALT and BERR lines will both be driven and the processor attempts to rerun the cycle. This mode is normally not useful because the same bus error will presumably reoccur.

3.3 DTACK Select

The DTACK generator consists of a 74164 shift register that is held in its cleared state until either LDS or UDS is asserted. Logic ones are clocked through the shift register by the 16 MHz LOCO II oscillator, and the DTACK timing is selected by choosing the stage of the shift register connected to the DTACK input pin. DTACK delays that are available are given below. These times are measured from the onset of the data strobe until DTACK is asserted. Notice that the DTACK timer is active only for on-board memory accessses. For off-board accesses DTACK is derived from the Multibus XACK signal.

Jumper	DTACK Delay
A	85 ns
B	150 ns
C	215 ns
D	280 ns
E	345 ns
F	410 ns
G	475 ns
H	540 ns

3.4 Interrupt Priority Wiring

No interrupts are connected by traces on the printed circuit board. Each interrupt must be wired to the priority encoder as needed. Interrupts from the on-board peripheral chips are each terminated on individual wire wrap posts. Because Motorola IRQ lines are open drain connections, the interrupt requests from several chips may be wired ORed to occupy a single priority level.

The Multibus interrupt lines (8) are each terminated on a wire wrap post. These may also be wire ORed and connected to the priority encoder inputs.

Priority encoder input seven is the highest priority; one is the lowest. Interrupt requests are not latched on-board. They must be held active until serviced when they are reset by the processor during execution of the interrupt service routine.

3.5 CCLK and BCLK

Jumpers J1 and J2, when installed, connect the on-board 10 MHz oscillator to the Multibus CCLK and BCLK lines, respectively. For a single processor system these jumpers should be in place. For multi-processor systems, only one master should drive the Multibus clock lines. Removing the jumpers removes the clock from the bus.

3.6 Bus Arbitration

Two jumpers are associated with the bus priority logic. J3 connects the output of the bus arbitration logic to the Multibus BPRO/signal. J4 connects the BPRN/ line to ground. In a system with a single bus master J4 should be installed. In a Multibus system using serial priority, BPRN/ is driven by the BPRO/signal from the master with the next highest priority.

3.7 Initialize

Jumper J11 allows the reset line generated by this board to drive the INIT/ line of the Multibus bin. This jumper would usually be installed, but in some cases it may be desirable to reset the computer without reinitializing other Multibus cards.

3.8 Memory Socket Configuration

Several jumpers are associated with each pair of memory sockets to accommodate the various compatible RAM and ROM chips. Figure 3.2 defines the connections for each pin of the configuration jumpers. Figure 3.3 shows the jumpers installed for each memory type.

3.9 Timer

The timer (MC6840) has a clock, a gate and an output for each of its three timing channels. All nine of these signals are terminated on wire wrap pins. To operate the 6840 timer channels the gate signals must be low. A trace on the bottom side of the board connects each of the three gate signals to ground. A trace must be cut for the appropriate channel if the gate is to be operated from an active source.

To use the timer as a programmable interrupt generator for the CPU, no external clock or gate connections are needed. The 6840 may use the 800 kHz "E" clock as a time base. The timer IRQ is usually connected to a selected priority interrupt level.

4.0 Connector Pinouts

4.1 Multibus P1 and P2 Connectors

P1 is the Multibus connector - it is included for completeness. See Figure 4.1. The Multibus auxiliary connector P2 has only one active signal - the external reset line on pin 38. A low level on this pin or a contact closure between pin 38 and ground (pins 1,2,21, or 22) will cause a reset of the 68000.

On the original Intel Multibus user connectors, the pinout is defined contrary to the numbering of commercially available ribbon connectors. User connections on this board are numbered so that even pins are on the component side. This numbering is such that the pin number is the same as the wire number in a ribbon cable and mates with

the corresponding number on commercially available ribbon connectors. Notice that this is different from Intel numbering and we feel it is more consistent.

4.2 PIA and ACIA Connectors

In the following figures both the card edge pin and the "D" pin are shown for each signal on the PIA and ACIA connectors, because a 25 pin D connector is normally installed on the user end of the ribbon cable.

Signal	Pin No.		Pin No.		Signal
	"D"	Edge	Edge	"D"	
PA0	1	1	2	14	PA1
PA2	2	3	4	15	PA3
PA4	3	5	6	16	PA5
PA6	4	7	8	17	PA7
PB0	5	9	10	18	PB1
PB2	6	11	12	19	PB3
PB4	7	13	14	20	PB5
PB6	8	15	16	21	PB7
CA1	9	17	18	22	CB1
CA2	10	19	20	23	CB2
	11	21	22	24	
5 Volts	12	23	24	25	5 Volts
GND	13	25	26		GND

Figure 4.2 PIA connector

Signal	Pin No.		Pin no.		Signal
	"D"	Edge	Edge	"D"	
GND	1	1	2	14	
RX DATA	2	3	4	15	
TX DATA	3	5	6	16	
CTS	4	7	8	17	
RTS	5	9	10	18	
RTS	6	11	12	19	
GND	7	13	14	20	DCD
RTS	8	15	16	21	
	9	17	18	22	
	10	19	20	23	
	11	21	22	24	
	12	23	24	25	
	13	25	26		

Figure 4.3 ACIA Connector

5.0 Memory Decoding

Multibus defines 20 address lines on the backplane. Although the 68000 can support 24 bits of address, the upper four bits are ignored making an available address space of 1 Megabyte. Memory allocation is programmable through the use of Programmable Array Logic (PAL) circuits.

5.1 Memory and I/O Decoding PALS

Figure 5.1 shows the schematic of the decoding method. The first level of decoding is done in a 12L6 PAL that has as inputs A19-A12, FC2, FC1, FC0, and AS. Outputs from the 12L6 are:

MS1 - An enable for the memory select PAL

MS0 - A memory select output to indicate a restart access.

FBIO - off-board I/O access.

FBM - off-board memory access.

NBIO - on-board I/O.

NBM - on-board memory access. Used to initiate the DTACK generator.

With the configuration described above an individual output pin can be asserted for blocks of addresses as small as 4K (A12 is the lowest address input). This means that on-board I/O and off-board I/O will each consume 4K of address space.

When the 68000 is reset, it fetches a supervisor stack pointer and an initial value for the program counter from memory locations 0 through 7. Because no assumption can be made about the contents of RAM at reset time, the restart vectors must be fixed in PROM. Other exception and interrupt vectors are located in memory locations 8 through 3FF, but it is convenient to have these vectors in RAM. The 68000 accesses restart vectors as supervisory program; other vectors as supervisory data. Using this distinction we can cause the memory decoder to direct restart vector accesses to PROM and other vector accesses to RAM. It is for this reason that two enable signals, MS0 and MS1, are generated by the 12L6 decoder.

The 12L6 uses the 68000's address strobe, AS, as a chip enable so that no outputs will be asserted unless a valid address is on the bus.

A second PAL selects the socket pairs labeled MEM0, MEM1...MEM7 on the board. A 10L8 PAL is used here with one output for each socket pair. Inputs to the 10L8 are MS0, MS1, A10...A17. This configuration allows an on-board address space of up to 256K bytes. Individual memory select assignments can be as small as 1K blocks (A10 is the lowest address line input to the 10L8).

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For an on-board I/O access, the NBIO pin of the 12L6 PAL becomes the chip select for the I/O select 74S287 PROM. Inputs to the 74S287 are A8...A1 so an output pin may be asserted for as few as two contiguous memory locations. The four output lines of the I/O select PROM are used to select the Host ACIA, Terminal ACIA, timer and the PIA's. Both PIA's are selected by pin 9 of the 74S287, but an additional PIA select (CS0) is activated by UDS.VMA, LDS.VMA for PIA0 and P1A1. This design allows byte access to either PIA or word access to both PIA's together.

The NBIO signal is the 68000 VPA input signal. When VPA is asserted the 68000 synchronizes its data transfer with its own E clock. During an interrupt acknowledge, FC0, FC1, and FC2 are asserted. This condition is detected and the NBIO output becomes active to provide a VPA signal to the processor. This causes a fetch of the interrupt autovector requested by the interrupt priority encoder. Note that a conflict can exist if a I/O device is selected during an interrupt acknowledge cycle. This problem can only occur if I/O device addresses are stored in the top eight locations of the I/O select PROM. These locations should be left unprogrammed. (See Figure 5.8.)

5.2 Example Memory Map

An example of a memory map for the 68000 computer board is shown in Figure 5.2. In this design RAM is placed in the first 8K of memory using MK4118 (1KX8) RAM chips. Space is provided to change to MK4802 (2KX8) RAM chips. RAM is placed in memory socket pairs MEM0,1, 2, 3. A 4K block of off-board memory is located at $4000 - $4FFF (to be used as video RAM) followed by two 4K byte blocks of I/O space for on-board and off-board I/O at $5000 and $6000, respectively.

At $10000 a 64K block is allocated for off-board memory and at $20000 and above, 8K blocks of on-board memory are allocated for memory socket pairs MEM7,6,5,4,3 and 2. Note that sockets MEM2 and MEM3 are allocated both for 1K RAM between $1000 and $1FFF and for 4KX8 (2532) PROM between $28000 and $2BFFF. This arrangement allows those sockets to be used for either type of memory as needed.

5.3 PAL Logic Equations

The PAL logic equations that define this memory map and the corresponding hex format needed to program the PAL devices, are given in Figures 5.3 through 5.6. These figures are computer output from the PAL assembler program supplied by Monolithic Memories Incorporated.

5.4 I/O Address Assignments

Figure 5.7 shows a typical assignment of the address space for the on-board peripherals. The base address is determined by the 12L6 PAL and the least significant addresses are assigned by programming the 256 x 4 I/O select PROM. Figure 5.8 shows the data stored in the I/O PROM for the address assignments of Figure 5.7.

68K Multibus On-Board I/O

On-Board I/O Base Address = $5000

AC1A1:	5001	Status/Control
	5003	Data Reg.
AC1A2:	5021	Status/Control
	5023	Data Reg.
P1A1:	5041	A Data Register
	5043	B Data Register
	5045	A Control Register
	5047	B Control Register
P1A2:	5040	A Data Register
	5042	B Data Register
	5044	A Control Register
	5046	B Control Register
Timer:	5061	Control Reg. No. 1 and No. 3
	5063	Control Reg. No. 2 Status Reg.
	5065	MSB Timer 1
	5067	LSB
	5069	MSB Timer 2
	506B	LSB
	506D	MSB Timer 3
	506F	LSB

Figure 5.7 On-Board I/O Address Assignments

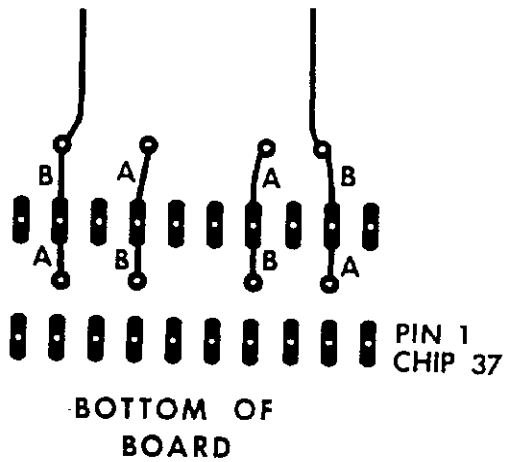
5.5 The 16L8 PAL Option

The PAL devices come in various levels of complexity to fit the application. The 12L6 and the 10L8 chips described here are the least complex of the PAL devices. A PAL is really a programmable array of AND gates that connect to a fixed OR gate for each output pin. Because of their internal structure these devices are faster than most bipolar PROMS and the outputs do not exhibit the glitches generated by a true PROM memory chip. However, for each variety of PAL, there is a fixed limit to the number of different configurations of input data

that can be specified to assert a given output pin. In the 10L8 there are two inputs to the internal OR gate that drives each output. For the 12L6, four outputs have two terms; two outputs have four terms. The outputs with four terms are connected MS1 and NBM.

The result of the above discussion is that four separate blocks of on-board memory may be specified; two independent blocks of Multibus memory; each memory socket pair may be accessed as two different addresses etc.

If a more complicated memory map is needed, more ways of asserting a given output pin are needed. A more complex memory map is possible if a 16L8 PAL is substituted for the simpler types. The 16L8 provides seven separate product terms for asserting each output pin.



cut at "A" (4 plcs.) for PAL12L6

cut at "B" (4 plcs.) for PAL16L8

Figure 5.9 PAL 12L6/16L8 Cut Trace Option

The 16L8 will directly replace the 10L8, but two input and output pins must be swapped to accommodate the 16L8 in a 12L6 socket. The layout of this board provides for using either PAL type through cut trace options on the solder side of the board near the address Decode PAL socket (chip 37). Figure 5.9 shows the location of these cut trace options on the solder side of the board. Notice that four cuts are required regardless of which PAL is used.

5.6 68000 Memory Organization

Motorola and Intel processors store 16-bit words with the high and low bytes in the opposite order. Intel words are stored with the least significant byte at even byte addresses and the most significant byte in the next higher (odd) location. This organization was inflicted on Multibus memory and peripheral cards by defining a 16-bit transfer to have the even byte asserted on data lines D0 - D7; odd bytes on D8 - D15.

The 68000 memory organization places the most significant byte in even addresses; least significant bytes at the next higher (odd) addresses.

The design criterion placed on this computer card was that bytes placed in byte addresses will be stored at the proper location in memory, and those data, read as 16-bit words, will appear at the 68000 in the correct order. To achieve this goal a swap byte buffer arrangement is needed on the CPU card. This design is shown in Figure 5.10.

Notice that for byte transfers, no problem exists. The bytes are transferred on D0 - D7 as expected. Only the 16-bit transfers are affected in which case Multibus lines D0 - D7 carry the data that will arrive at the 68000 as the most significant byte D8 - D15; a similar swap is made for the least significant byte.

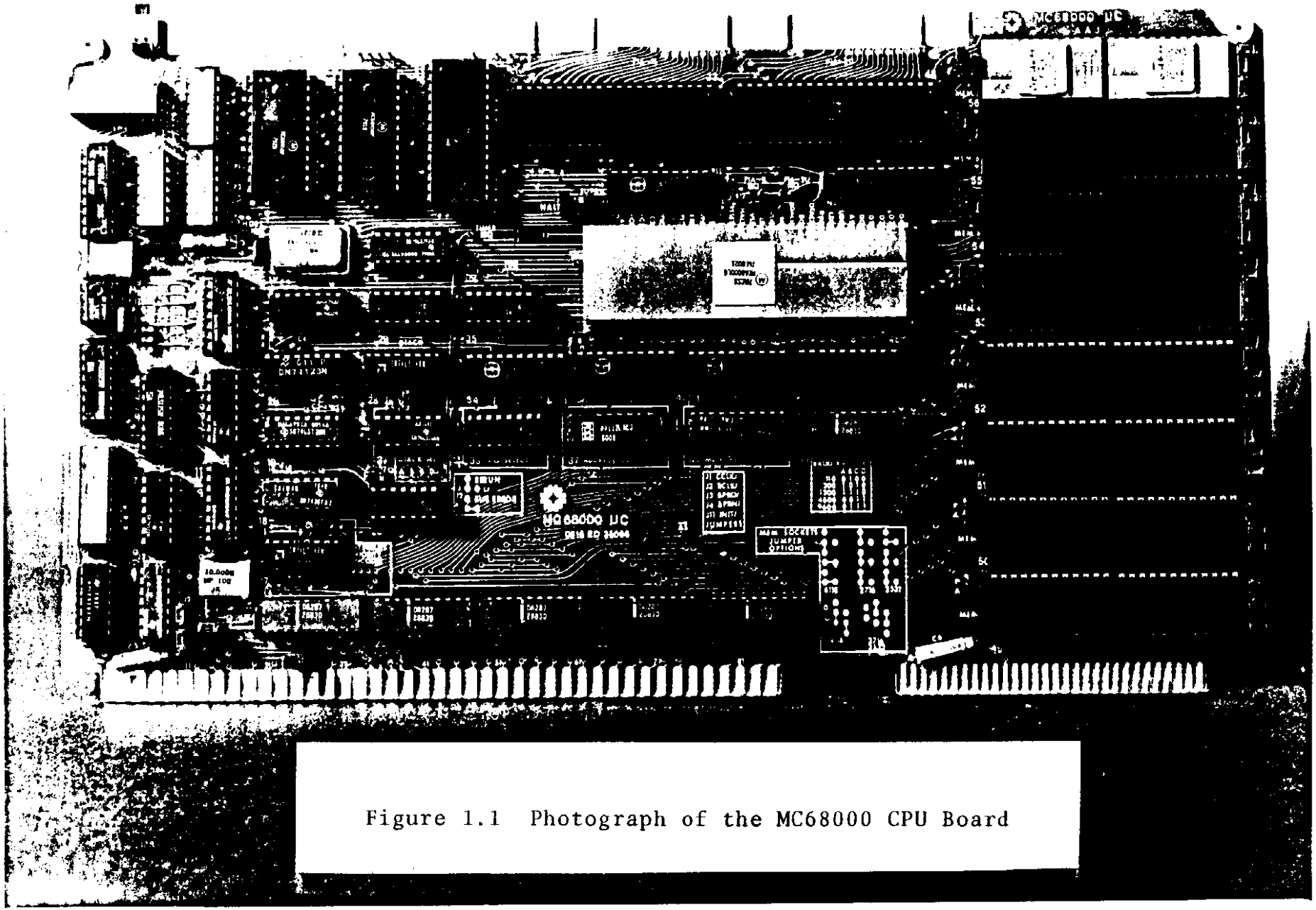


Figure 1.1 Photograph of the MC68000 CPU Board

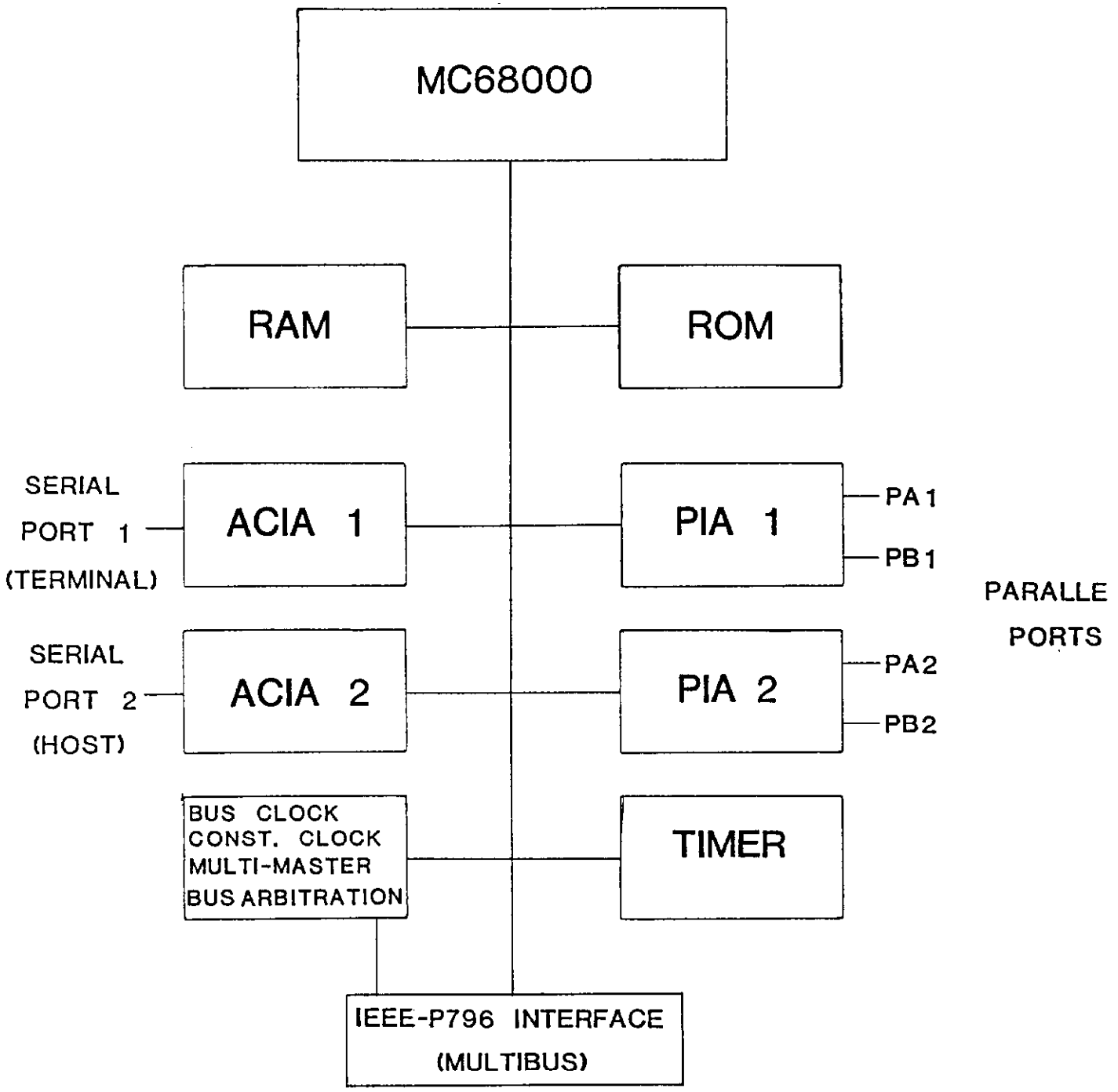
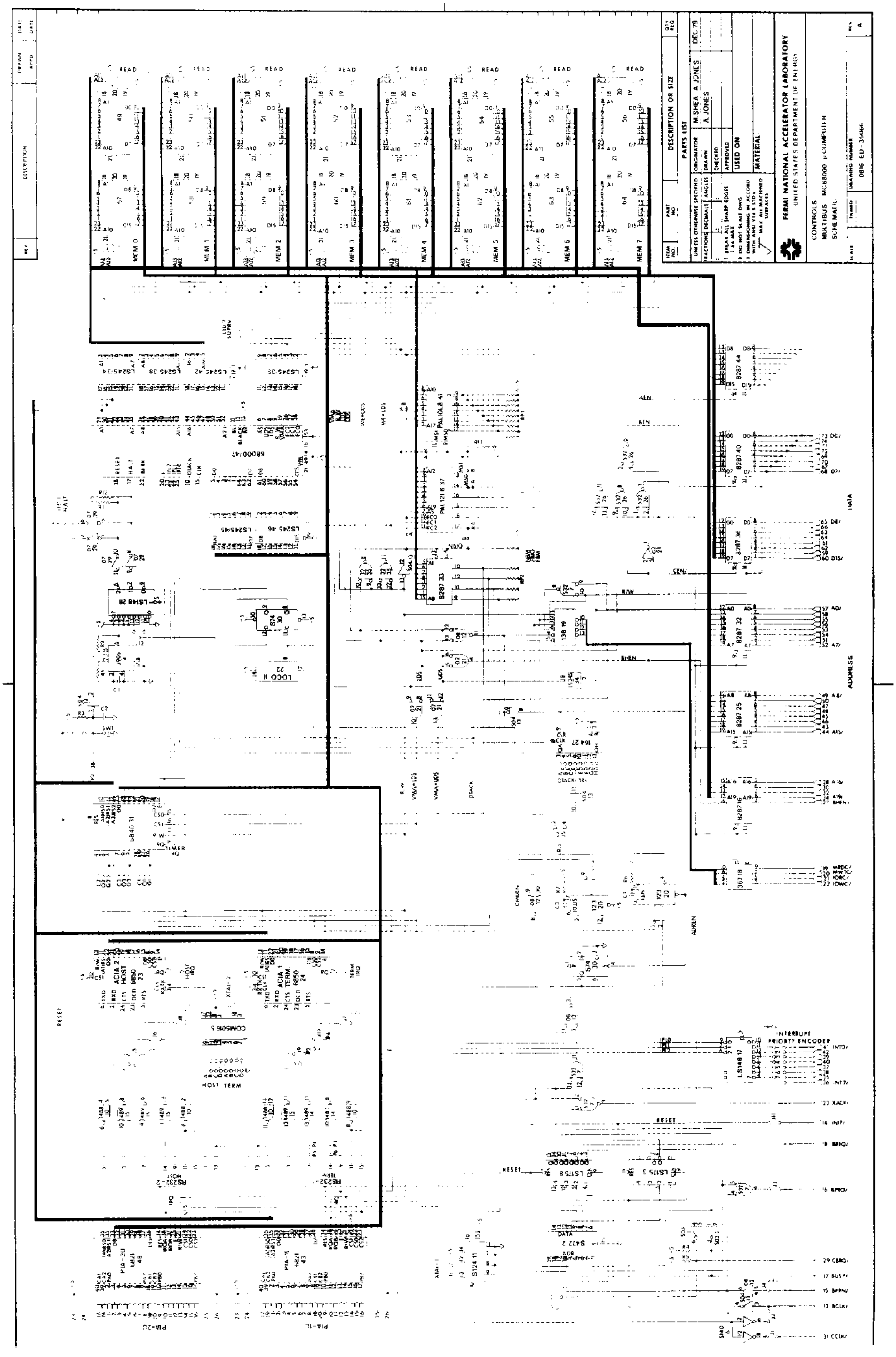


Figure 1.2 Block Diagram of the MC6800 CPU Board


FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY
CONTROLS
MULTIBUS MC68000 µCOMPUTER
SCHEMATIC
0816 ED-35066
PARTS LIST
DESCRIPTION OR SIZE
M. SHEA A. JONES
A. JONES
DEC 79
USED ON
MATERIAL
MEM 0
MEM 1
MEM 2
MEM 3
MEM 4
MEM 5
MEM 6
MEM 7
READ
DATA
ADDRESS
INTERRUPT
PRIORITY ENCODER
RESET
HOST TERM

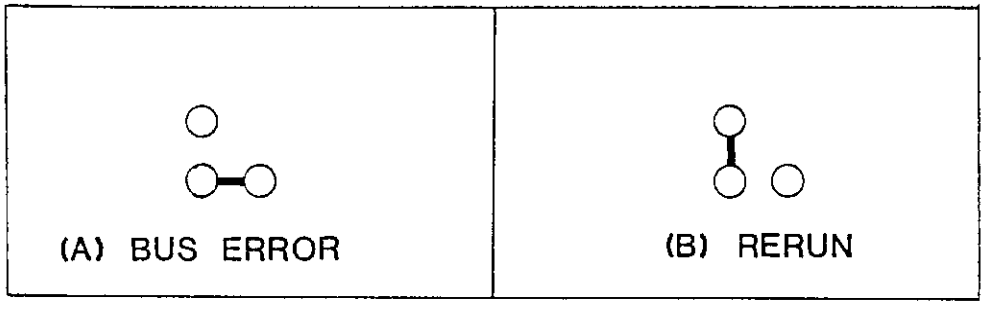


Figure 3.1 BERR Jumper Configuration

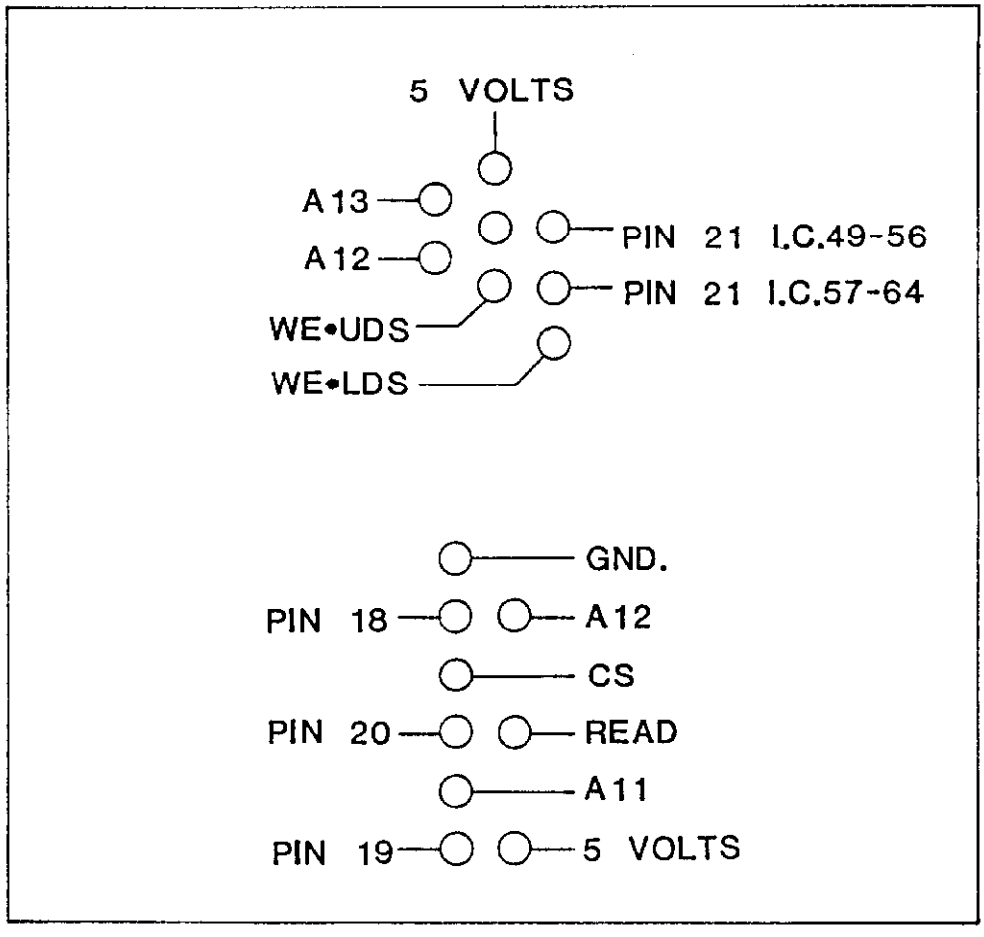


Figure 3.2 Memory Socket Jumper Connections

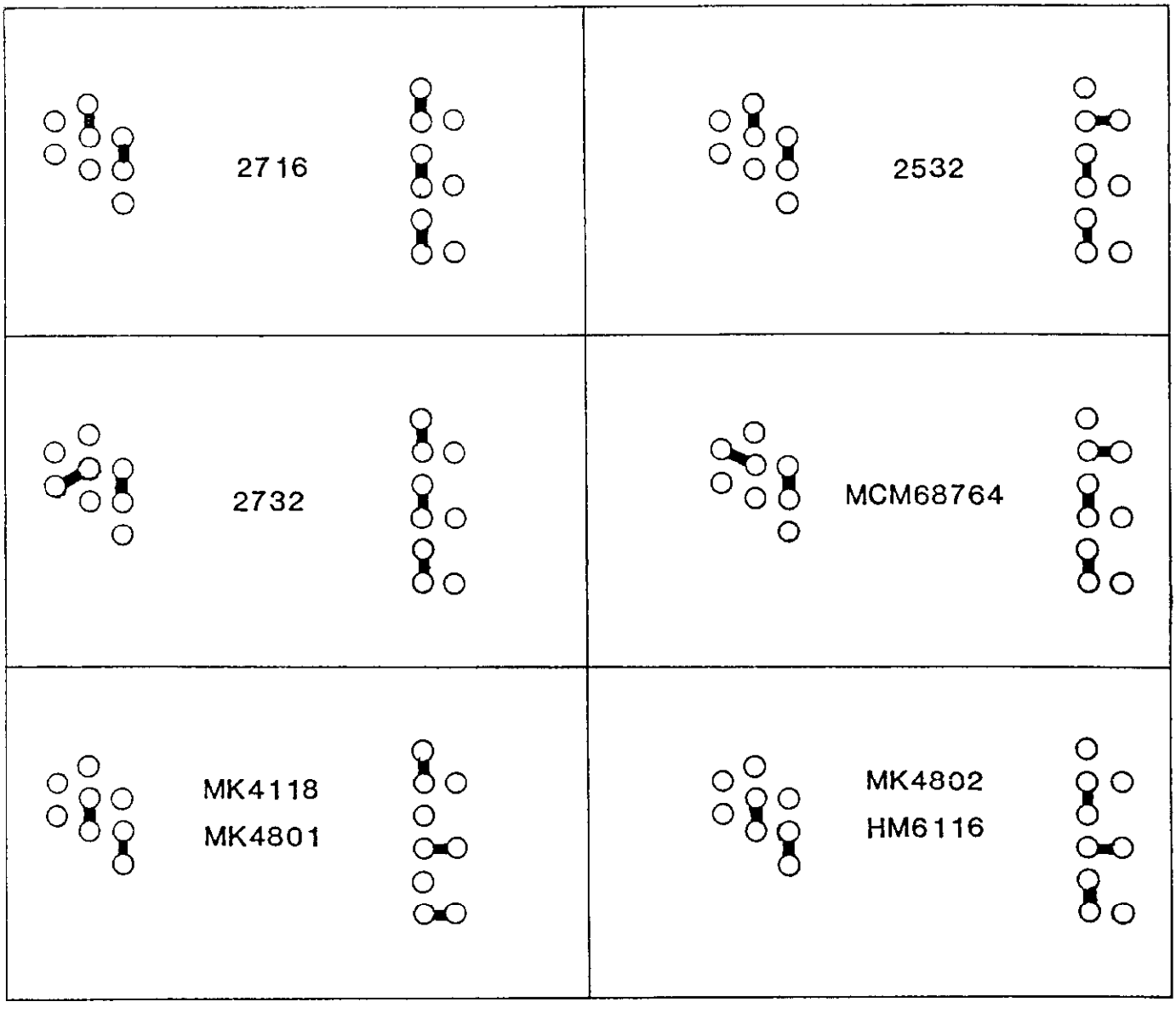


Figure 3.3 Jumpers for Various Memory Types

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Sig GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9	-5V	-5Vdc	10	-5V	-5Vdc
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 disable RAM
BUS CONTROLS AND ADDRESS	25		Reserved	26	INH2/	Inhibit 2 disable PROM or ROM
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Intr Acknowledge	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

Figure 4.1 Multibus P1 Connector Pinout

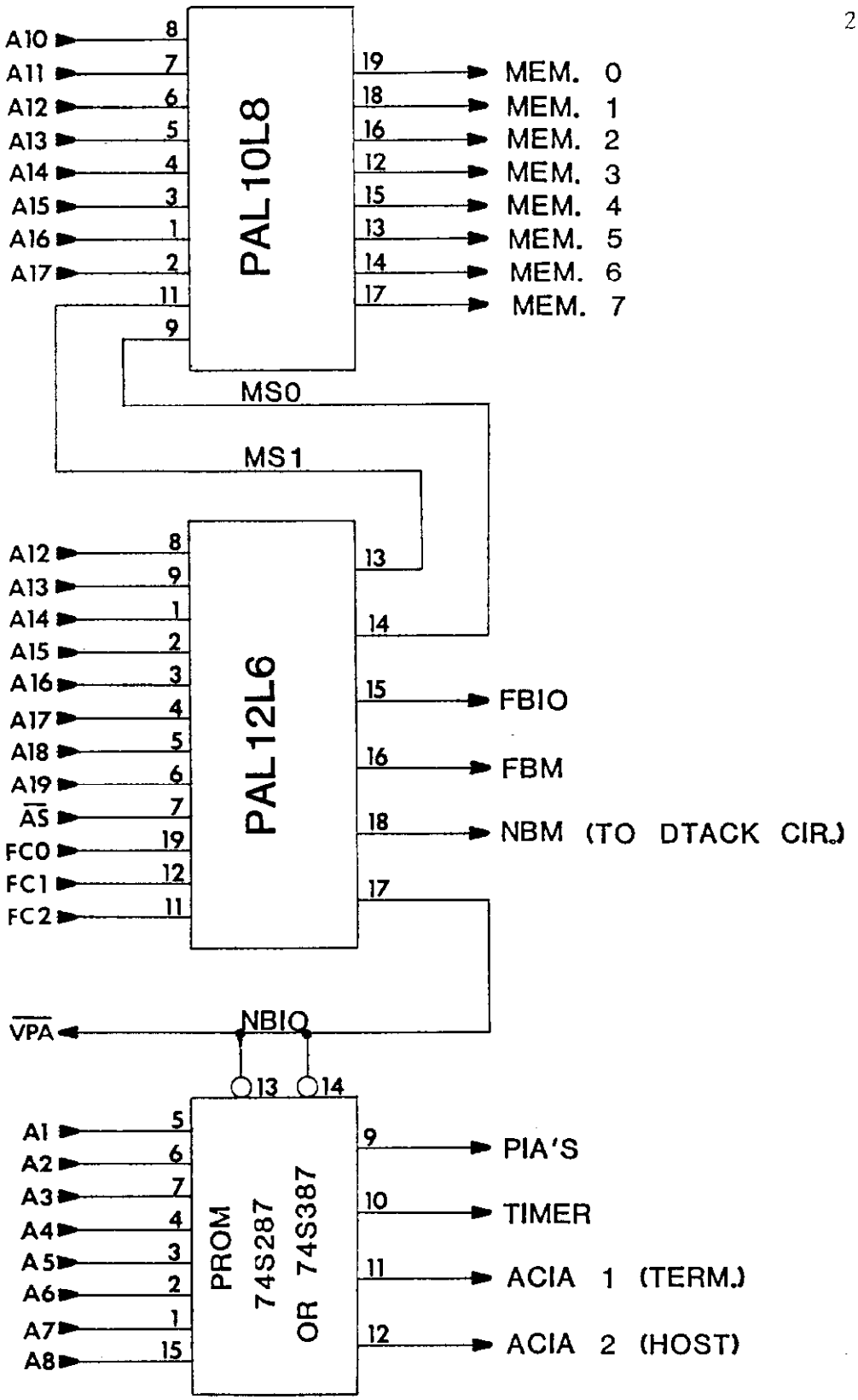


Figure 5.1 Memory Decoding Diagram

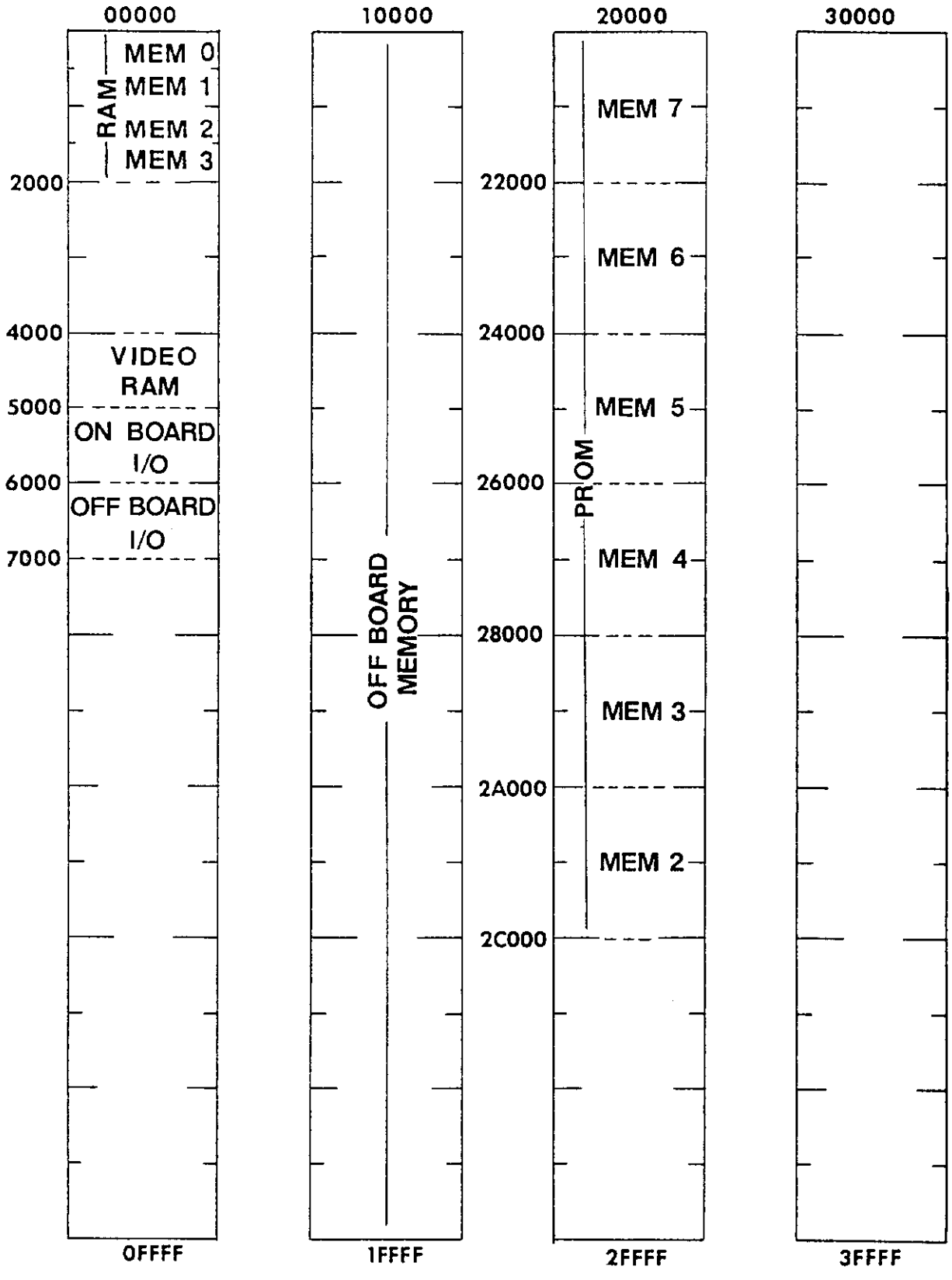


Figure 5.2 Example Memory Map

```
PALASMB

PAL12L6 ADDRESS DECODE FOR 68000 MULTIBUS SINGLE BOARD MICRO-P
LINAC MEMORY MAP          9/5/80

A14 A15 A16 A17 A18 A19 AS A12 A13 GND
FC2 FC1 MS1 MS0 FBI0 FBM NBI9 NBM FC0 VCC


NBI9=/AS*/A19*/A18*/A17*/A16*/A15*A14*/A13*A12
     +/AS*FC0*FC1*FC2*A19*A18*A17*A16*A15*A14*A13*A12
FBI9=/AS*/A19*/A18*/A17*/A16*/A15*A14*A13*/A12
FBM=/AS*/A19*/A18*/A17*/A16*/A15*A14*/A13*/A12
    +/AS*/A19*/A18*/A17*A16
NBM=/AS*/A19*/A18*/A17*/A16*/A15*/A14*/A13
    +/AS*/A19*/A18*A17*/A16
MS0=FC2*FC1*/AS*/A19*/A18*/A17*/A16*/A15*/A14*/A13*/A12
MS1=/AS*/A19*/A18*/A17*/A16*/A15*/A14*/A13
    +/AS*/A19*/A18*A17*/A16
```

Figure 5.3 PAL12L6 Design Equations

```
HEX FORMAT FOR PROGRAMER

LINAC MEMORY MAP          9/5/80
E 0 2 C E 0 E E E 0 E E E 0 E E E 0 E E E 0 E E A 6 E E E 0 E E
A E A E 2 C A E 8 6 E E A 4 E E A 4 E E E 0 E E A E A E A E A E
0 0 0 0 0 0 0 0 0 0 2 2 0 0 2 2 0 0 2 2 0 0 2 2 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 2 2 0 0 2 2 0 0 2 2 0 0 2 2 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 0 6 1 7 0 7 7 7 0 7 7 7 0 7 7 7 0 7 7 7 0 7 7 7 4 5 7 6 1 5 7
4 4 4 4 4 0 4 4 0 4 7 7 4 0 7 7 4 0 7 7 4 0 7 7 4 4 4 4 4 4 4 4
0 0 0 0 0 0 0 0 0 0 4 4 0 0 4 4 0 0 4 4 0 0 4 4 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 4 4 0 0 4 4 0 0 4 4 0 0 4 4 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

Figure 5.4 PAL12L6 Hex Format

```
PAL10L8 MEMORY SELECT FOR 68000 MULTIBUS SINGLE BOARD MICRO-P
LINAC MEMORY MAP          9/5/80

A16  A17  A15  A14  A13  A12  A11  A10  MS0  GND
MS1  MEM3 MEM5 MEM6 MEM4 MEM2 MEM7 MEM1 MEM0 VCC


MEM0=/MS1*MS0*/A17*/A16*/A15*/A14*/A13*/A12*/A11*/A10
     +/MS1*/A17*/A16*/A15*/A14*/A13*/A12*/A11*A10
MEM1=/MS1*/A17*/A16*/A15*/A14*/A13*/A12*A11
MEM2=/MS1*/A17*/A16*/A15*/A14*/A13*A12*/A11
     +/MS1*A17*/A16*A15*/A14*A13
MEM3=/MS1*/A17*/A16*/A15*/A14*/A13*A12*A11
     +/MS1*A17*/A16*A15*/A14*/A13
MEM4=/MS1*A17*/A16*/A15*A14*A13
MEM5=/MS1*A17*/A16*/A15*A14*/A13
MEM6=/MS1*A17*/A16*/A15*/A14*A13
MEM7=/MS1*/MS0*/A17*/A16*/A15*/A14*/A13*/A12*/A11*/A10
     +/MS1*A17*/A16*/A15*/A14*/A13
```

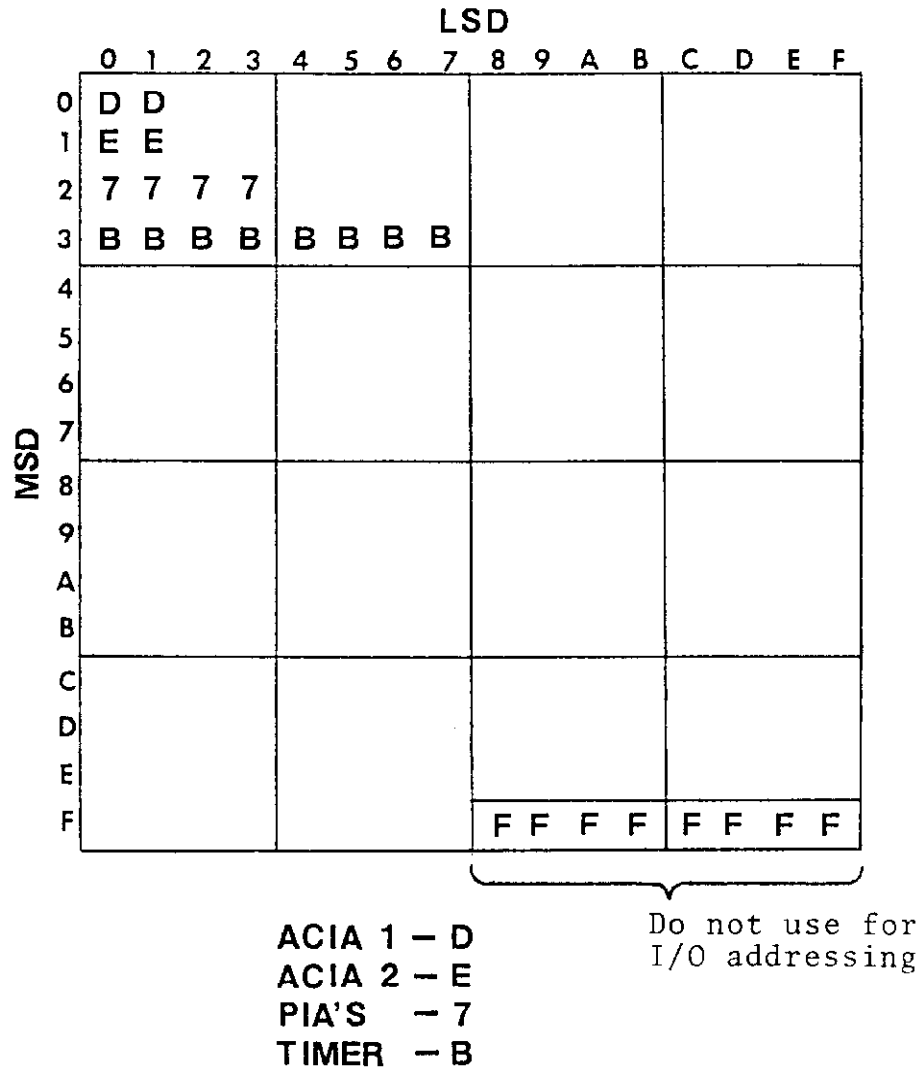
Figure 5.5 PAL10L8 Design Equations

```
HEX FORMAT FOR PROGRAMER

LINAC MEMORY MAP          9/5/80
     F0 F0 F0 FF F0 FF 78 FF D2 FF FA FF EB F0
     1C D0 58 FF D0 F5 8F FD CF FD CF CD FF DD 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     87 F0 F0 FA 5F FC 3F F7 FF F7 FF FF FF FF F0
     08 80 08 FF 80 FF 80 FF 80 FF 80 FF 80 80 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
     00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

Figure 5.6 PAL10L8 Hex Format

I/O SELECT PROM MEMORY MAP



Note: All unused locations should contain $F

Figure 5.8 I/O PROM Data

BHEN/	ADR0/	MULTIBUS TRANSFER DATA PATH	DEVICE BYTE TRANSFERRED	16-BIT DEVICE	MULTIBUS	68000 CPU BOARD	MC68000
H	H	8-BIT, DAT0/ - DAT7/	EVEN	LOW, EVEN BYTES HIGH,ODD BYTES	DAT0/ - DAT7/ DAT8/ - DATF/		D0—7 UDS D8—F
H	L	8-BIT, DAT0/ - DAT7/	ODD	LOW, EVEN BYTES HIGH,ODD BYTES	DAT0/ - DAT7/ DAT8/ - DATF/		D0—7 LDS D8—F
L	H	16-BIT, DAT0/ - DATF/	EVEN AND ODD	LOW, EVEN BYTES HIGH, ODD BYTES	DAT0/ - DAT7/ DAT8/ - DATF/		D0—7 LDS UDS D8—F

Figure 5.10 cpu Board Data Bus Buffer Arrangement